

WHAT IS CLAIMED IS:

1. A reusable software block adapted to control multiple instantiations of a peripheral device within a system, the reusable software block
5 comprising:
- a device hardware abstraction layer defining offset values for registers of the peripheral device and defining a data structure for the peripheral
10 device; and
 - a platform hardware abstraction layer defining an address map of the system, the platform hardware abstraction layer adapted to initialize each
15 instantiation of the peripheral device via calls to the device hardware abstraction layer.
2. The reusable software block of claim 1
20 wherein the device hardware abstraction layer comprises:
- memory registers adapted to be configurable during initialization; and
 - interrupt connections adapted to be
25 configurable during initialization.
3. The reusable software block of claim 2
wherein the memory registers and the interrupt connections define the data structure of the
30 peripheral device using variables.

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4. The reusable software block of claim 1 wherein the data structure of the peripheral device is defined in the device hardware abstraction layer
5 using variables, the memory map comprising:

memory locations associated with each
instantiation of the peripheral
device.

10 5. The reusable software block of claim 1 wherein the platform hardware abstraction layer initializes each memory location according to the memory map.

15 6. The reusable software block of claim 1 wherein the data structure of the peripheral device is defined in the device hardware abstraction layer using variables, the platform hardware abstraction layer comprising:

20 an interrupt configuration corresponding to
interrupt connections for a particular
implementation of the peripheral
device.

25 7. The reusable software block of claim 6 wherein the platform hardware abstraction layer initializes each interrupt connection of the particular implementation of the peripheral device according to the interrupt configuration.

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8. A method of initializing multiple instances of a peripheral device within an integrated circuit, the method comprising:

5 coding a peripheral device in a device hardware abstraction layer, the coded peripheral device representing a functional and behavior model of a circuit element independent of the
10 integrated circuit;
mapping the peripheral device of the device hardware abstraction layer onto the integrated circuit for each instantiation of the peripheral
15 device.

9. The method of claim 8 wherein each instantiation of the peripheral device is modified programmatically from the basic structure during
20 mapping.

10. The method of claim 8 wherein the step of mapping comprises:
defining parameters for each instance of
25 the peripheral device module; and
instantiating each instance of the peripheral device module using the defined parameters to modify the

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variable parameters of the basic structure.

11. The method of claim 8 wherein the basic
5 structure comprises:

variable base addresses of memory registers
in an integrated circuit; and
variable locations of interrupt connections
in an integrated circuit.

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12. The method of claim 8 wherein the step of
coding comprises:

defining base addresses of registers and
interrupt location of interrupt
15 connections within the basic structure
as variables within the device
hardware abstraction layer.

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13. The method of claim 8 wherein the step of
20 mapping comprises:

initializing registers of the peripheral
device using an initialization
function defined within the peripheral
device module, the initialization
25 function adapted to receive a memory
location and to initialize the
registers of the peripheral device
with the memory location.

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14. The method of claim 8 wherein the method is performed using ANSI C Code.

15. The method of claim 8 wherein the peripheral device is coded using a command to construct a structure representative of register locations for each instantiation of the peripheral device.

10 16. A system for instantiating multiple instances of a peripheral device within an integrated circuit using a single configurable code block, the system comprising:

15 a device hardware abstraction layer defining a configurable structure for the peripheral device; and
a platform hardware abstraction layer adapted to configure the structure of each particular instantiation of the peripheral device via the device hardware abstraction layer.

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17. The system of claim 16 wherein the device hardware abstraction layer comprises:

25 memory registers adapted to be configurable during initialization; and
interrupt connections adapted to be configurable during initialization.

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18. The system of claim 17 wherein the memory registers and the interrupt connections define the structure of the peripheral device using variables.

5 19. The system of claim 16 wherein the configurable structure of the peripheral device is defined in the device hardware abstraction layer using variables, the platform hardware abstraction layer comprising:

10 a memory map of memory locations of the peripheral device corresponding to a particular implementation of the peripheral device, the memory map adapted to replace the variables with
15 unique memory locations for each instantiation.

20. The system of claim 16 wherein the configurable structure of the peripheral device is
20 defined in the device hardware abstraction layer using variables, the platform hardware abstraction layer comprising:

an interrupt configuration corresponding to
interrupt connections for a particular
25 implementation of the peripheral device, the interrupt configuration adapted to replace the variables with unique interrupt connections for each instantiation.